REMARKS

The following remarks are made in response to the Non-Final Office Action mailed November 7, 2005. In that Office Action, the Examiner rejected claim 1 under 35 U.S.C. §102(e) as being anticipated by Keeth et al., U.S. Patent No. 6,807,114 ("Keeth"). Claims 2, 3, 5-9, 11-15, and 17 were rejected under 35 U.S.C. §103(a) as being unpatentable over Keeth and Cowles et al., U.S. Patent No. 6,556,497 ("Cowles").

The Examiner's indication that claim 18 is allowed, and that claims 4, 10, and 16 (although objected to) would be allowable if re-written, is noted with appreciation.

With this Response, claims 10 and 16 have been amended. Claims 1-18 remain pending in the application and are presented for reconsideration and allowance.

35 U.S.C. §102 Rejections

On pages 2 and 3 of the Office Action, the Examiner rejected claim 1 under 35 U.S.C. §102(e) as being anticipated by Keeth. The Examiner indicated that Keeth teaches a dynamic random access memory device capable of converting from a full density memory device to a reduced density memory device to compensate for cell failures in a plurality of cell blocks. The Examiner indicated that Keeth discloses a row address mapping fuse, citing Figure 1 and element 51, which is a fuse bank, for selectively determining row address combinations void of cell failures and capable of storing data bits, citing column 4, lines 40-61. Further, the Examiner indicated that Keeth discloses row address mapping logic, citing Figure 2, element 52, which is a column select circuit, coupled to the row address mapping fuse, citing column 5, lines 62-67 and column 6, lines 1-58.

Applicant respectfully disagrees with the Examiner's position regarding disclosure within Keeth. In particular, Keeth does not teach, show, or suggest a dynamic random access memory device capable of converting from a full density memory device to a reduced density memory device, as claimed in independent claim 1. Rather, Keeth discloses a redundant scheme which includes a redundancy circuit, as well as redundant rows and columns of memory cells to replace defective memory cells. Specifically, Keeth states "Figure 1 is a block diagram of a conventional synchronous dynamic random access memory ("SDRAM") 2 that utilizes a

conventional redundant column technique as described above. However, as explained below, the SDRAM 2 can be modified to use **redundant** column techniques according to various embodiments of the invention, which can also be used with memory devices other than the SDRAM 2." See Keeth at column 3, lines 52-58. Furthermore, with reference to SDRAM 2' of Figure 2 of Keeth, "[a] decoded column signal CDEC selecting a defective column of memory cells is redirected to the next lower numbered column (or to the redundant column), as are all decoded column signals." See Keeth at column 6, lines 10-15. This prior art solution is specifically discussed in the present application at page 2, lines 3-9.

In the approach disclosed in Keeth, the size of the memory, which is presented to an external circuit, is always the same independent of whether redundant columns or rows are substituted for defective columns or rows. In a memory device utilizing a redundant scheme, such as disclosed in Keeth, conversion from a full density memory device to a reduced density memory device is not performed. Therefore, the corresponding memory device of Keeth is not capable of converting from a full density memory device to a reduced density memory device, as claimed in independent claim 1.

Applicant respectfully requests that the rejection of independent claim 1 under 35 U.S.C. §102(e) be withdrawn.

35 U.S.C. §103 Rejections

On pages 3-8 of the Office Action, the Examiner rejected claims 2, 3, 5-9, 11-15, and 17 under 35 U.S.C. §103(a) as being unpatentable over Keeth and Cowles. Regarding independent claims 8 and 14, the Examiner indicated that Keeth teaches a method of converting a full density memory device to a reduced density memory device and includes selectively determining a reduced density address combination having address which omit cell blocks having cell block failures, citing column 5, lines 19-61. The Examiner further indicated that storing data bits at an address is disclosed, citing Keeth at column 6, lines 9-15, within the reduced density column address combination, citing Cowles a column 4, lines 31-61. The Examiner further indicated that it would have been obvious to a person of ordinary skill in the art to combine Keeth with Cowles, wherein the motivation for doing so would have been a flexibility of density modes, so

that the DRAM can be used in a full density mode or a half density mode based on the user's need. This assessment is respectfully traversed.

A full density mode or half density mode is not chosen based on the user's need, but due to defective memory cells. In other words, the reduced density mode is provided correct the problem of defective memory cells. Conversely, as previously discussed with reference to claim 1 above, Keeth solves the problem of defective memory cells by making use of a redundancy scheme rather than conversion from a full density mode to a half density mode. The mode of memory is not capable of changing in Keeth. The size of memory of Keeth, which is presented to an external circuit, does not change, regardless of whether redundant columns or rows are substituted for defective columns or rows. A person skilled in the art does not have any motivation to modify the Keeth system so that a memory device is capable of converting from a full density memory device to a reduced density memory device is obtained since Keeth discloses a redundant scheme, rather than a half density mode, to accommodate for defective memory cells. In other words, there is no motivation to combine Cowles and Keeth, since each reference is attempting to deal with defective memory cells by utilizing different, opposing solutions. Further, the combination of Keeth and Cowles would result in a non-functioning memory device.

With respect to claim 2, the Examiner indicated that the row address multiplexer 18 of Keeth is disclosure of a multiplexer having a first input coupled to a reduced density enable signal, a second input coupled to a logic value setting signal, and a third input coupled to a row address. However, it is clear from Figure 1 of Keeth that row address multiplexer 18 comprises two inputs only, one connected to address register 12 and one connected to refresh counter 30. Thus, the row address multiplexer 18 of Keeth can clearly not represent the multiplexer defined in claim 2 of the present application. Moreover, as previously explained, a person skilled in the art does not have any motivation to combine the teachings of Keeth and Cowles. In addition, there is no teaching or suggestion why one would provide row address multiplexer 18 of Keeth with a further input for receiving a reduced density enable signal, since Keeth does not discuss a reduced density enable signal.

Applicant respectfully requests that the rejection of claims 2, 3, 5-9, 11-15, and 17 under 35-U.S.C. §103(a) be withdrawn.

Objected to and Allowed Claims

On page 8 of the Office Action, the Examiner indicated that claim 18 is allowed. The Examiner further indicated that claims 4, 10, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if re-written in independent form including all of the limitations of the base claim and any intervening claims. With this Response, claims 10 and 16 have been re-written in independent form including all of the limitations of the base claim and any intervening claims. Claim 4 has not been amended; however, claim 4 depends from claim 2, which depends from independent claim 1. As previously discussed, it is believed that independent claim 1 is patentably distinguishable over the cited art.

Applicant respectfully requests the allowance of claims 4, 10, and 16.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 1-18 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 1-18 is respectfully requested.

Applicants hereby authorize the Commissioner for Patents to charge Deposit Account No. 50-0471 in the amount of **$400.00** to cover the fees as set forth under 37 C.F.R. 1.16(h).

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to Michael R. Binzak at Telephone No. (612) 573-0427, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

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CERTIFICATE UNDER 37 C.F.R. 1.8:

The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, as first class mail, in an envelope address to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 7th day of **February**, 2006.

By:
Name: **Michael R. Binzak**